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Confirmation No. 8452

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant:	TERECHKO *et al.*	Examiner:	Cao, C.
Serial No.:	10/561,625	Group Art Unit:	2115
Filed:	December 19, 2005	Docket No.:	NL021505 US
Title:	ARRANGEMENT AND METHOD FOR CONTROLLING POWER MODES OF HARDWARE RESOURCES		

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence and the papers, as described hereinabove, are being transmitted via facsimile-Formal Entry, to the attention of the Examiner at Commissioner for Patents, MAIL STOP APPEAL BRIEF, P.O. Box 1450, Alexandria, VA 22313-1450, on August 30, 2007.

By: Kelly J. Ledin

Facsimile No.: 571 273-8300

APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Customer No. 65913

Dear Sir:

This Appeal Brief is submitted pursuant to 37 C.F.R. §41.37, in support of the Notice of Appeal filed June 30, 2007 and in response to the rejections of claims 1-30 as set forth in the Final Office Action dated April 10, 2007, and in further response to the Advisory Action dated May 23, 2007.

Please charge Deposit Account number 50-0996 (NXPS.208PA) $500.00 for filing this brief in support of an appeal as set forth in 37 C.F.R. §1.17(c). If necessary, authority is given to charge/credit Deposit Account 50-0996 additional fees/overages in support of this filing.

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I. Real Party In Interest

The real party in interest is NXP Semiconductors. The application is presently assigned of record, at reel/frame nos. 017403/0010 to Koninklijke Philips Electronics, N.V., headquartered in Eindhoven, the Netherlands. We have been authorized by both the assignee of record and NXP Semiconductors to convey herein that the entire right, title and interest of the instant patent application has been transferred to NXP Semiconductors.

II. Related Appeals and Interferences

While Appellant is aware of other pending applications owned by the above-identified Assignee, Appellant is unaware of any related appeals, interferences or judicial proceedings that would have a bearing on the Board's decision in the instant appeal.

The undersigned has recently been made aware of a similar application, U.S. Application No. 10/561,627 to Terechko *et al.* and filed on Dec. 3, 2003. While the undersigned is not aware of any appeals, interferences or judicial proceedings in relation to this application, the undersigned was made aware of a number of references for this similar application. The undersigned has not performed a review these references and is unaware of any specific teachings that are relevant to the present appeal. Accordingly, this disclosure is made in an abundance of caution and is not intended to be an admission as to the relevance of the references.

III. Status of Claims

Claims 1-30 stand rejected and claims 1-17 and 19-30 are presented for appeal. Pursuant to 37 C.F.R. § 41.33, Appellant requests that claim 18 be cancelled without prejudice for possible future inclusion of related subject matter through amendment.

A complete listing of the claims under appeal is provided in an Appendix to this Brief.

IV. Status of Amendments

The only amendment filed subsequent to the Office Action dated April 10, 2007 is the present request to cancel claim 18.

V. Summary of Claimed Subject Matter

Commensurate with independent claim 1, an example embodiment of the present invention is directed to a circuit arrangement, comprising: (a) a plurality of hardware resources (*See, e.g.*, FIG. 2, elements 58 and 60), wherein each hardware resource has a power mode configurable between at least first and second power consumption states; and (b) a processor (*See, e.g.*, FIG. 1, element 14) coupled to the plurality of hardware resources, the processor configured to process program code that includes at least one power control instruction (*See, e.g.*, FIG. 4, element 90) that includes an operand having power control information disposed therein (*See, e.g.*, FIG. 4, elements 94, 97 and 98), wherein the processor is configured to process the power control instruction by selectively setting power modes of at least two hardware resources among the plurality of hardware resources based upon the power control information disposed in the power control instruction (*See, e.g.*, page 5, lines 10-15), and wherein the processor is further configured to maintain the power modes of the at least two hardware resources to that specified in the power control instruction while processing at least one subsequent instruction in the program code (*See, e.g.*, page 5, lines 10-15).

Commensurate with independent claim 19, an example embodiment of the present invention is directed to a method of executing program code on a processor (*See, e.g.*, FIG. 1, element 14) coupled to a plurality of hardware resources (*See, e.g.*, FIG. 2, elements 58 and 60), each having a power mode configurable between at least first and second power consumption states (*See, e.g.*, page 5, lines 3-9), the method comprising: (a) processing a power control instruction (*See, e.g.*, FIG. 4, element 90) from the program code by selectively setting power modes of at least two hardware resources among the plurality of hardware resources (*See, e.g.*, page 5, lines 10-15) based upon power control information disposed in an operand of the power control instruction (*See, e.g.*, FIG. 4, elements 94, 97 and 98); and (b) processing at least one subsequent instruction in the program code while the power modes of the at least two hardware resources are set to that specified by the power control information of the power control instruction (*See, e.g.*, page 5, lines 10-15).

Commensurate with independent claim 27, an example embodiment of the present invention is directed to a method of generating program code for execution by a processor (*See, e.g.*, FIG. 1, element 14) coupled to a plurality of hardware resources (*See, e.g.*, FIG. 2, elements 58 and 60), each having a power mode configurable between at least first and second power consumption states (*See, e.g.*, page 5, lines 3-9), the method comprising: (a) analyzing at least a portion of a program to determine utilization of the plurality of hardware resources by the processor during execution of at least a section of program code from the program (*See, e.g.*, page 6, lines 4-27); (b) based upon the determined utilization of the plurality of hardware resources, inserting a power control instruction into the program (*See, e.g.*, page 6, lines 4-27), the power control instruction including power control information disposed in an operand (*See, e.g.*, FIG. 4, elements 94, 97 and 98) thereof that specifies power modes for at least two hardware resources among the plurality of hardware resources, wherein the power control instruction is configured to be executed prior to at least one non-power control instruction in the program code, and wherein the program code is configured to cause the processor to dynamically set the power modes for the at least two hardware resources to that specified in the power control instruction such that the non-power control instruction will be processed while the power modes of the at least two hardware resources are maintained at that specified in the power control instruction (*See, e.g.*, page 5, lines 10-15).

As required by 37 C.F.R. § 41.37(c)(1)(v), a concise explanation of the subject matter defined in the independent claims involved in the appeal is provided herein. Appellant notes that representative subject matter is identified for these claims; however, the abundance of supporting subject matter in the application prohibits identifying all textual and diagrammatic references to each claimed recitation. Appellant thus submits that other application subject matter, which supports the claims but is not specifically identified above, may be found elsewhere in the application. Appellant further notes that this summary does not provide an exhaustive or exclusive view of the present subject matter, and refers to the specification, including the appended claims and their legal equivalents, for additional example embodiments.

VI. Grounds of Rejection to be Reviewed Upon Appeal

A. Whether claims 1-9, 11-17 and 19-30 are unpatentable under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,307,281 to Houston (Houston).

B. Whether claim 10 is unpatentable under 35 U.S.C. 103(a) as being obvious over U.S. Patent No. 6,307,281 to Houston (Houston) in view of U.S. Publication No. 2003/0177482 to Dinechin (Dinechin).

VII. Argument

A. The rejections of Claims 1-9, 11-17 and 19-30 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,307,281 to Houston (Houston)

i. The rejections of claims 1-9, 11-17 and 19-30 under 35 U.S.C. 102(b) are improper because Houston reference does not teach each claim limitation.

The rejections are improper because the Examiner has not addressed each claim limitation and because the unaddressed claim limitations are not taught by the Houston reference. The law is clear that for a claim to anticipate a reference, it must teach each element of the claim. *See, e.g.*, M.P.E.P. 2131 citing to *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987). The claimed inventions of each of independent claims 1, 19 and 27 include limitations directed to the use of power control information that is stored in an operand. These uses of an operand are valuable to facilitating a number of embodiments of the present invention. Moreover, the dependent claims, separately addressed in the subsequent section, include further limitations that cover different uses of the data from the operand, according to various embodiments of the invention. *See, e.g.*, FIG. 4 of Appellant's specification. The record clearly shows that the Houston reference does not mention any use of data stored in an operand. In fact, the Houston reference fails to mention or allude to the use of an operand in any capacity. The record shows that Appellant's repeated discussion of this failure has largely been ignored by the Examiner. The latest Advisory Action provides an indication that the Examiner's failure is likely due an erroneous assumption that a power control instruction is the same as an operand. More specifically, in the Advisory Action of May 23, 2007 the Examiner

erroneously equates an operand with an instruction: "Houston discloses a program code having power control instructions with an operand (power control instructions)..." This erroneous assumption ignores claim limitations of the present invention.

Consistent with Appellant's disclosure, instructions are often identified by an opcode (*e.g.*, 92 of FIG. 4 of Appellant's Disclosure). An operand, however, is a separate, data carrying portion of an instruction (*e.g.*, elements 94 and 97 of FIG. 4 and page 13, lines 18 *et al.* of Appellant's Disclosure), which is not a necessary portion of all instructions. As such, an operand with power control information is clearly not synonymous with, nor an inherent part of, an instruction, power-control or otherwise. Appellant notes that the claim limitations clearly identify limitations directed toward a power control instruction that is further limited to have the claimed operand with power control information. Accordingly, because the Houston reference does not teach each element and the Examiner's assumption that an instruction is the same as an operand is erroneous, the rejection does not meet the standards of a 35 U.S.C 102(b) rejection. Accordingly, the 35 U.S.C. Section 102(b) rejections of claims 1-9, 11-17 and 19-30 must be reversed.

ii. <u>The rejections of claims 3-7, 13 and 21-24 under 35 U.S.C. 102(b) are improper because Houston reference does not teach each claim limitation.</u>

With reference to the discussion of the previous section, the discrepancy between the Examiner's assertion and the teachings of the Houston reference is magnified in the Examiner's assertions relative to various dependent claims, many of which discuss various uses of the power control information from the operand. As the Houston reference does not teach any such operand, the Examiner's interpretation of each dependent claim creates further confusion as to how the Houston reference is being asserted as corresponding to the claim limitations.

Each of claims 3-7, 13 and 21-24 include various limitations directed to setting the power modes by using an external register to that stores the power control information from the operand of the power control instruction or that is identified by this power control

information. Further limitations regarding the association between the operand and various other aspects of various embodiments of the invention are also found in these claims. For instance, the asserted correspondence to claims 6 and 7, in which the operand is used to provide enable information for enabling/disabling banks of registers, is allegedly found in FIGs. 6, 7 and 9 of the Houston reference and the discussion thereof. *See, i.e.,* Final Office Action, April 10, 2007 at page 5. Apparently, the Examiner is asserting that the registers 76 and/or 86 are taught to be enabled/disabled. The Houston reference, however, does not teach that these registers are disabled/enabled. Instead, these registers are taught to hold enable information for enabling/disabling a completely different element (*e.g.*, element 70 and/or element 80). Thus, in order for the registers to function as the Examiner has asserted, the registers would need to enable/disable themselves. Appellant submits that this would be illogical and nonfunctional because once the register was disabled it would cease to provide the enable/disable information to itself. Thus, the register would either remain indefinitely disabled or immediately transition back to an enabled state. Accordingly, due to the Houston reference's failure to teach the use of an operand with power control information, the Examiner's assertion of correspondence to such further limitations is also illogical, and thus, Appellant is unable to further address the propriety of those rejections.

In summary, neither the Examiner's citations nor Appellant's review of the Houston reference reveals any portion of the Houston reference that teaches power control instructions that include operands with power control information. Accordingly, the 35 U.S.C. Section 102(b) rejections of claims 3-7, 13 and 21-24 must be reversed.

B. The rejections of claim 10 under 35 U.S.C. 103(a) as being obvious over U.S. Patent No. 6,307,281 to Houston (Houston) in view of U.S. Publication No. 2003/0177482 to Dinechin (Dinechin)

The Section 103(a) rejection of the dependent claim 10 (which depends from claim 1), must also be reversed in view of the above discussion regarding the independent claim rejections and the improper reliance upon the Houston reference. That is, where an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *See, e.g., In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988). In this regard, further

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discussion of claim 10 is unnecessary and the rejections must be reversed in view of the above discussion.

VIII. Conclusion

In view of the above, Appellant submits that the rejections of claims 1-17 and 19-30 are improper. Appellant therefore requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the undersigned's deposit account was provided on the first page of this brief.

Please direct all correspondence to:

Corporate Patent Counsel
NXP Intellectual Property & Standards
1109 McKay Drive; Mail Stop SJ41
San Jose, CA 95131

CUSTOMER NO. 65913

Respectfully Submitted,

By: _____
Name: Robert J. Crawford
Reg. No.: 32,122
Tel: 651 686-6633 ext. 101
(NXPS.208PA)

APPENDIX OF CLAIMS INVOLVED IN THE APPEAL
(S/N 10/538,104)

1. A circuit arrangement, comprising: (a) a plurality of hardware resources, wherein each hardware resource has a power mode configurable between at least first and second power consumption states; and (b) a processor coupled to the plurality of hardware resources, the processor configured to process program code that includes at least one power control instruction that includes an operand having power control information disposed therein, wherein the processor is configured to process the power control instruction by selectively setting power modes of at least two hardware resources among the plurality of hardware resources based upon the power control information disposed in the power control instruction, and wherein the processor is further configured to maintain the power modes of the at least two hardware resources to that specified in the power control instruction while processing at least one subsequent instruction in the program code.

2. The circuit arrangement of claim 1, wherein the power control instruction includes an opcode that uniquely identifies the power control instruction.

3. The circuit arrangement of claim 1, further comprising: (a) a support register that stores power modes state information for the plurality of hardware resources; and (b) enabling logic coupled to the support register and configured to control the power modes of the plurality of hardware resources responsive to the power modes state information stored in the support register, wherein the processor is configured to selectively set the power modes of the at least two hardware resources by storing the power control information from the power control instruction in the support register.

4. The circuit arrangement of claim 3, wherein the support register comprises a power modes register.

5. The circuit arrangement of claim 3, wherein the support register includes additional status information that is unrelated to power dissipation control.

6. The circuit arrangement of claim 3, wherein a subset of the plurality of hardware resources comprises a plurality of banks of registers defining a register file, wherein the enable logic includes a plurality of enable circuits, each associated with a bank of registers from the plurality of banks of registers, and each configured to selectively disable its associated bank of registers responsive to an enable signal, wherein the enable logic is further configured to generate the enable signal for each bank of registers from the power modes state information stored in the support register.

7. The circuit arrangement of claim 6, wherein each bank of registers includes at least one clock input, address input and data input, and wherein the enable circuit for each bank of registers is configured to selectively gate off the clock, address and data inputs for its associated bank of registers in response to the enable signal provided thereto.

8. The circuit arrangement of claim 1, wherein each hardware resource is selected from the group consisting of a register file, a register bank, a register, a cache, a bus interface unit, a bus, a functional unit, a functional block and an instruction decoder.

9. The circuit arrangement of claim 1, wherein the processor is configured to process explicitly parallel instructions, and wherein the power control instruction comprises an operation among a plurality of operations in an explicitly parallel instruction.

10. The circuit arrangement of claim 9, wherein the processor is selected from the group consisting of a VLIW processor and an EPIC processor.

11. The circuit arrangement of claim 1, wherein the processor comprises a superscalar processor.

12. The circuit arrangement of claim 1, wherein the processor is configured to assign a side effect to the power control instruction to limit run-time speculation thereof.

13. The circuit arrangement of claim 1, wherein the power control information in the operand identifies a register within which power modes state information for the at least two hardware resources is stored, and wherein the processor is configured to selectively set the power modes of the at least two hardware resources by retrieving the power modes state information from the register identified by the power control information in the operand.

14. The circuit arrangement of claim 1, wherein the plurality of hardware resources are disposed in the processor.

15. The circuit arrangement of claim 1, wherein at least one hardware resource is disposed outside of the processor but on the same integrated circuit as the processor.

16. The circuit arrangement of claim 1, wherein at least one hardware resource is disposed on a separate integrated circuit from the processor.

17. An integrated circuit comprising the circuit arrangement of claim 1.

18. (Cancelled).

19. A method of executing program code on a processor coupled to a plurality of hardware resources, each having a power mode configurable between at least first and second power consumption states, the method comprising: (a) processing a power control instruction from the program code by selectively setting power modes of at least two hardware resources among the plurality of hardware resources based upon power control information disposed in an operand of the power control instruction; and (b) processing at least one subsequent instruction in the program code while the power modes of the at least two hardware resources are set to that specified by the power control information of the power control instruction.

20. The method of claim 19, wherein the power control instruction further includes an opcode that uniquely identifies the power control instruction.

21. The method of claim 19, wherein the processor includes a support register that is utilized by enable logic in the processor to set the power modes of the plurality of hardware resources, and wherein selectively setting the power modes of at least two hardware resources includes storing the power control information in the support register.

22. The method of claim 21, further comprising, after processing the first subsequent instruction, processing a second power control instruction from the program code by storing second power control information disposed in an operand thereof in the support register such that the power mode of a first hardware resource is modified, and processing a second subsequent instruction after processing the second power control instruction, whereby the second subsequent instruction is processed while the power mode of the first hardware resource is set to that specified in the second power control instruction.

23. The method of claim 21, wherein a subset of the plurality of hardware resources comprises a plurality of banks of registers defining a register file, wherein the enable logic includes a plurality of enable circuits, each associated with a bank of registers from the plurality of banks of registers, and each configured to selectively disable its associated bank of registers responsive to an enable signal, the method further comprising generating the enable signal for each bank of registers from the power modes state information stored in the support register.

24. The method of claim 23, wherein each bank of registers includes at least one clock input, address input and data input, and wherein the enable circuit for each bank of registers is configured to selectively gate off the clock, address and data inputs for its associated bank of registers in response to the enable signal provided thereto.

25. The method of claim 19, wherein each hardware resource is selected from the group consisting of a register file, a register bank, a register, a cache, a bus interface unit, a bus, a functional unit, a functional block and an instruction decoder.

26. The method of claim 19, wherein the processor is configured to process explicitly parallel instructions, and wherein the power control instruction comprises an operation among a plurality of operations in an explicitly parallel instruction.

27. A method of generating program code for execution by a processor coupled to a plurality of hardware resources, each having a power mode configurable between at least first and second power consumption states, the method comprising: (a) analyzing at least a portion of a program to determine utilization of the plurality of hardware resources by the processor during execution of at least a section of program code from the program; (b) based upon the determined utilization of the plurality of hardware resources, inserting a power control instruction into the program, the power control instruction including power control information disposed in an operand thereof that specifies power modes for at least two hardware resources among the plurality of hardware resources, wherein the power control instruction is configured to be executed prior to at least one non-power control instruction in the program code, and wherein the program code is configured to cause the processor to dynamically set the power modes for the at least two hardware resources to that specified in the power control instruction such that the non-power control instruction will be processed while the power modes of the at least two hardware resources are maintained at that specified in the power control instruction.

28. The method of claim 27, wherein analyzing the program and inserting the power control instruction are performed during at least one of compilation and optimization of the program.

29. The method of claim 27, wherein analyzing the program and inserting the power control instruction are performed concurrently with execution of the program by the

processor.

30. The method of claim 27, further comprising consolidating resource usage in the program to a limited subset of hardware resources prior to inserting the power control instruction into the program.

APPENDIX OF EVIDENCE

Appellant is unaware of any evidence submitted in this application pursuant to 37 C.F.R. §§ 1.130, 1.131, and 1.132.

APPENDIX OF RELATED PROCEEDINGS

As stated in Section II above, Appellant is unaware of any related appeals, interferences or judicial proceedings.